42390.P3187R PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of	)
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Albert Fazio	)Examiner: Unassigned
	)
Patent No.: 5,742,543	)Art Unit: Unassigned
	)
Issued: April 21, 1998	)
	)
For: A FLASH MEMORY DEVICE OF CAPABLE OF SENSING A THRESHOLD VOLTAGE OF MEMORY CELLS ON A PAGE MODE OF OPERATION	)

Box: Reissue
Assistant Commissioner for Patents
Washington, D.C. 20231

REISSUE APPLICATION

Sir:

Applicants respectfully request entry of the following claim amendments:

"Express Mail" mailing label number: EL867649029US

Date of Deposit: February 21, 2002

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Beverly Kehoe Shea
(Typed or printed name of person mailing paper or fee)

Beverly Kehoe Shea
(Signature of person mailing paper or fee)

February 21, 2002
(Date signed)

CLAIMS AS THEY STAND

The claims are included herewith for the Examiner's review. The unamended claims are marked "unamended", while amended claims are marked "amended".

1. (Unamended) A method for determining data stored by a memory cell having a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode couple to a conductor, comprising the steps of:

floating the bitline:

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell; and

sensing the third voltage to determine the data stored by the memory cell.

2. (Unamended) The method of claim 1, further comprising an initial step of setting the bitline to a ground potential.

3. (Unamended) The method of claim 1, wherein the memory cell is a nonvolatile memory cell.

4. (Unamended) A method for simultaneously determining data stored by a plurality of memory cells each having a select gate coupled to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor, comprising the steps of:

floating the plurality of bitlines;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells; and

sensing the plurality of third voltages to determine the data stored by the plurality of memory cells.

5. (Unamended) The method of claim 4, further comprising an initial step of setting the plurality of bitlines to a ground potential.

6. (Unamended) The method of claim 4, wherein the plurality of memory cells are nonvolatile memory cells.

7. (Unamended) The method of claim 4, wherein determining the data stored by the plurality of memory cells comprises reading a page of data.

8. (Unamended) A method for determining data stored by a memory cell having an adjustable threshold voltage, a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor, comprising the steps of:

floating the bitline;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitiline is set to a third voltage;

determining the adjustable threshold voltage of the memory cell based on the third voltage; and

determining the data stored in the memory cell based on the adjustable threshold voltage of the memory cell.

9. (Unamended) A memory device comprising:

a memory array having data stored in a memory cell, the memory cell having a select gate coupled to a wordline,

a first electrode coupled to a bitline, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell, wherein the periphery circuit sensing the third voltage to determine the data stored by the memory cell.

10. (Unamended) The memory device of claim 9, wherein the periphery circuit further transmits a ground potential to the bitline before transmitting the first voltage or the second voltage to the memory cell.

11. (Unamended) The memory device of claim 9, wherein the memory cell is a nonvolatile memory cell.

12. (Unamended) The memory device of claim 9, wherein the periphery circuit comprises:

a voltage regulation circuit outputting the first voltage and the second voltage;

a voltage switching circuit coupling the second voltage to the memory cell; and

a sensing circuit coupled to the memory cell, wherein the sensing circuit senses the third voltage to determine the data stored by the memory cell.

13. (Unamended) The memory device of claim 12, further comprising:

a decoder circuit receiving the first voltage from the voltage switching circuit and coupling their first voltage to the memory cell, the decoder circuit decoding a location of the memory cell in the memory array.

14. (Unamended) The memory device of claim 12, further comprising:

a control circuit having read circuitry and write circuitry each coupled to the voltage regulation circuit, the voltage switching circuit, and the sensing circuit, wherein the control circuit controls when the first voltage and the second voltage are supplied to the memory cell and when the third voltage is sensed by the sensing circuit.

15. (Unamended) The memory device of claim 12, wherein the sensing circuit comprises:

an analog-to-digital converter circuit operative to receive the third voltage and generate a digital value.

16. (Unamended) A memory device comprising:

a memory array having data stored in a plurality of memory cells, the plurality of memory cells each having a select gate couple to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells, and wherein the periphery circuit simultaneously sense the plurality of the third voltages to determine the data stored by the memory array.

17. (Amended) A memory device comprising:

a memory array having data stored in a memory cell having an adjustable threshold voltage; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a plurality of voltages comprising a first voltage and a second voltage to the memory cell and sensing the adjustable threshold voltage of the memory cell to determine the data stored by the memory cell based on a third voltage, the third voltage being equal to the first voltage minus a threshold voltage of the memory cell.

18. (Amended) A memory device comprising:

means having an adjustable threshold voltage for storing data; and

means coupled to the storing means for transmitting a first voltage and a second voltage to the storing means and for determining the data stored in the storing means by sensing the adjustable threshold voltage based on a third voltage, the third voltage being equal to the first voltage minus a threshold voltage of the storing means.

REMARKS

Status of Claims under 37 CFR 1.173(c)

Claims 1-16 stand as issued claims. Claims 17 and 18 have been amended.

Explanation of support under 37 CFR 1.173c

Support for applicant's amended claims is readily found in the specification of the U.S. Patent 5,742,543 (hereinafter "the '543 patent") in Figures 1-10 and the Specification, columns 3-8, for instance see Column 5, lines 23-42. The claims are for the same invention as that disclosed in the original patent, as required by 35 U.S.C 251.

Reason For Reissue

This reissue is filed because the patentee claimed more than he had a right to claims in the '543 patent. Issued claims 17 and 18 fail to cover certain embodiments of the invention with enough particularity to overcome prior art. The error arose during the drafting of the original application and during subsequent amendments in connection with the prosecution of the original application which resulted in the issuance of the patent. The errors arose without any deceptive intention on the part of the applicant.

Timeliness of the Reissue Application

The presented claim amendments narrow the scope of the issued claims and thus the reissue application is timely filed. This reissue application is being filed shortly after the applicant learned of the interference proceeding mentions below.

Concurrent Proceedings

The original patent is involved in an interference proceeding No. 104, 493. The patentee presently intends to file a motion under 37 C.F.R. 633 (h) to add the reissue application to the interference. The basis for the interference proceeding is a pending application, the specification of which is in U.S. Patent 5,095,344, which is prior art to the '543 patent.

Conclusion

The Applicant respectfully submits that the amended claims 17 and 18 do not add new matter and that all claims now pending are in condition for allowance and are patentably distinct over the U.S. Patent 5,095,344.

If there is a deficiency in fees, please charge our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 2/21/02

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AMENDED CLAIMS

Indicating Changes Made

17. (Amended) A memory device comprising:

a memory array having data stored in a memory cell having an adjustable threshold voltage; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a plurality of voltages comprising a first voltage and a second voltage to the memory cell and sensing the adjustable threshold voltage of the memory cell to determine the data stored by the memory cell based on a third voltage, the third voltage being equal to the first voltage minus a threshold voltage of the memory cell.

18. (Amended) A memory device comprising:

means having an adjustable threshold voltage for storing data; and

means coupled to the storing means for transmitting a first voltage and a second voltage to the storing means and for determining the data stored in the storing means by sensing the adjustable threshold voltage based on a third voltage, the third voltage being equal to the first voltage minus a threshold voltage of the storing means.